STM32MP15 peripherals overview

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SUMMARY

This article lists all internal peripherals embedded in STM32MP15 device and shows the assignment possibilities to the runtime contexts for each one of them.

Via this article, you can also access to individual peripheral articles in which information related to the overview and configuration can be found.

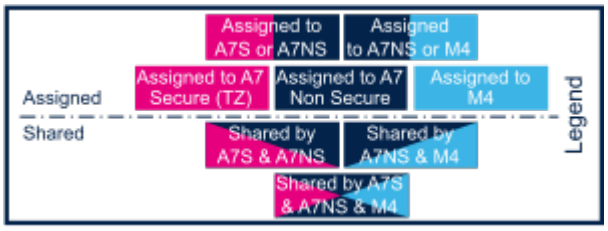
1 Internal peripherals overview

The figure below shows all **peripherals** embedded in STM32MP15 device, grouped per **functional domains** that are reused in many places of this wiki to structure the articles.

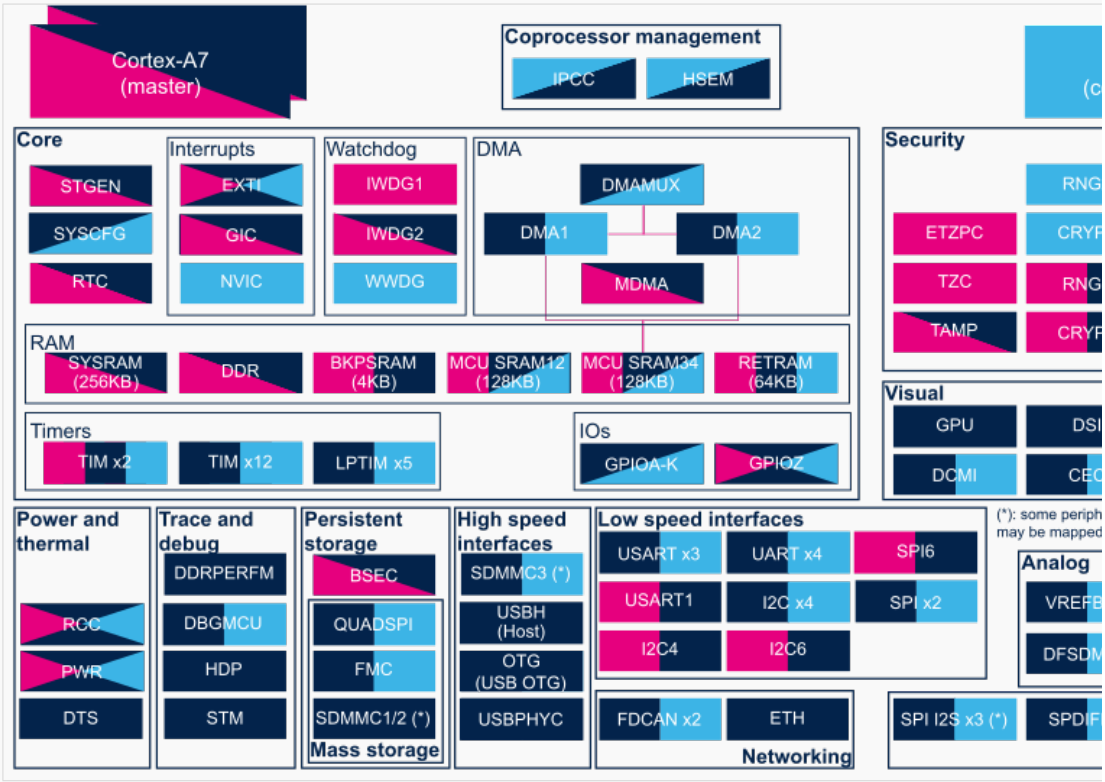
Several **runtime contexts** exist on STM32MP15 device[1], corresponding to the different **Arm cores and associated security modes**:

- Arm dual core Cortex-A7 secure (Trustzone), running a Secure Monitor or Secure OS like OP-TEE
- Arm dual core Cortex-A7 non secure, running Linux
- Arm Cortex-M4 (non-secure), running STM32Cube

Some peripherals can be strictly **assigned** to one runtime context: this is the case for most of the peripherals, like USART or I2C .
Other ones can be **shared** between several runtime contexts: this is the case for system peripherals, like PWR or RCC.
The legend below shows how assigned and shared peripherals are identified in the assignment diagram that follows:



Both the diagram below and the following summary table (in Internal peripherals assignment chapter below) are clickable in order to jump to each peripheral overview articles and get more detailed information (like software frameworks used to control them). They list STMicroelectronics recommendations. The STM32MP15 reference manual [2] may expose more possibilities than what is shown here.



STM32MP1 internal peripherals overview

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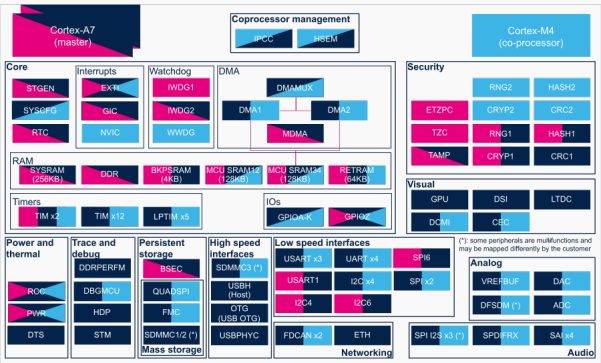
2 Internal peripherals assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- means that the peripheral can be assigned () to the given runtime context.
- is used for system peripherals that cannot be unchecked because they are statically connected in the device.

Refer to How to assign an internal peripheral to a runtime context for more information on how to assign peripherals manually or via STM32CubeMX.
The present chapter describes STMicroelectronics recommendations or choice of implementation. Additional possiblities might be described in STM32MP15 reference manuals .



Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Analog	ADC	ADC				Assignment (single choice)
Analog	DAC	DAC				Assignment (single choice)
Analog	DFSDM	DFSDM				Assignment (single choice)
Analog	VREFBUF	VREFBUF				Assignment (single choice)
Audio	SAI	SAI1				Assignment (single choice)
		SAI2				Assignment (single choice)
		SAI3				Assignment (single choice)
		SAI4				Assignment (single choice)
Audio	SPDIFRX	SPDIFRX				Assignment (single choice)

Domain	Peripheral	Runtime allocation				Comment
Coprocessor	IPCC	IPCC				Shared (none or both)
Coprocessor	HSEM	HSEM				
Core	RTC	RTC				RTC is mandatory to resynchronize ST GEN after exiting low -power modes.
Core	STGEN	STGEN				
Core	SYSCFG	SYSCFG				
Core/DMA	DMA	DMA1				Assignment (single choice)
		DMA2				Assignment (single choice)
Core/DMA	DMAMUX	DMAMUX				Shareable (multiple choices supported)
Core/DMA	MDMA	MDMA				Shareable (multiple choices supported)
Core /Interrupts	EXTI	EXTI				Shareable (multiple choices supported)
Core /Interrupts	GIC	GIC				
Core /Interrupts	NVIC	NVIC				
		GPIOA (16 pins)				Shareable (with pin granularity)
		GPIOB (16 pins)				Shareable (with pin granularity)
		GPIOC (16 pins)				Shareable (with pin granularity)
		GPIOD (16 pins)				Shareable (with pin granularity)
		GPIOE (16 pins)				Shareable (with pin granularity)
		GPIOF (16 pins)				Shareable (with pin granularity)
		GPIOG				Shareable (with pin

Domain	Peripheral	Runtime allocation				Comment
Core/IOs	GPIO	(16 pins)				granularity)
		GPIOH (16 pins)				Shareable (with pin granularity)
		GPIOI (16 pins)				Shareable (with pin granularity)
		GPIOJ (16 pins)				Shareable (with pin granularity)
		GPIOK (8 pins)				Shareable (with pin granularity)
		GPIOZ (8 pins)				Shareable (with pin granularity)
Core/RAM	BKPSRAM	BKPSRAM				Assignment (single choice)
Core/RAM	DDR via DDRCTRL	DDR				
Core/RAM	MCU SRAM	SRAM1				Assignment (between A7 S and A7 NS / M4) Shareable (between A7 NS and M4)
		SRAM2				Assignment (between A7 S and A7 NS / M4) Shareable (between A7 NS and M4)
		SRAM3				Assignment (between A7 S and A7 NS / M4) Shareable (between A7 NS and M4)
		SRAM4				Assignment (between A7 S and A7 NS / M4) Shareable (between A7 NS and M4)
Core/RAM	RETRAM	RETRAM				Assignment (single choice)

Domain	Peripheral	Runtime allocation				Comment
Core/RAM	SYSRAM	SYSRAM				Shareable (multiple choices supported)
Core/Timers	LPTIM	LPTIM1				Assignment (single choice)
		LPTIM2				Assignment (single choice)
		LPTIM3				Assignment (single choice)
		LPTIM4				Assignment (single choice)
		LPTIM5				Assignment (single choice)
Core/Timers	TIM	TIM1 (APB2 group)				Assignment (single choice)
		TIM2 (APB1 group)				Assignment (single choice)
		TIM3 (APB1 group)				Assignment (single choice)
		TIM4 (APB1 group)				Assignment (single choice)
		TIM5 (APB1 group)				Assignment (single choice)
		TIM6 (APB1 group)				Assignment (single choice)
		TIM7 (APB1 group)				Assignment (single choice)
		TIM8 (APB2 group)				Assignment (single choice)
		TIM12 (APB1				

Domain	Peripheral	Runtime allocation				Comment
		group)				Assignment (single choice)
		TIM13 (APB1 group)				Assignment (single choice)
		TIM14 (APB1 group)				Assignment (single choice)
		TIM15 (APB2 group)				Assignment (single choice)
		TIM16 (APB2 group)				Assignment (single choice)
		TIM17 (APB2 group)				Assignment (single choice)
Core /Watchdog	IWDG	IWDG1				
		IWDG2				Shared (none or both): • Cortex-A7 non secure for reload • Cortex-A7 secure for early interrupt handling
Core /Watchdog	WWDG	WWDG				
High speed interface	OTG (USB OTG)	OTG (USB OTG)				
High speed interface	USBH (USB Host)	USBH (USB Host)				
High speed interface	USBPHYC (USB HS PHY controller)	USBPHYC (USB HS PHY controller)				
		I2C1				Assignment (single choice)

Domain	Peripheral	Runtime allocation				Comment
		I2C2				Assignment (single choice)
		I2C3				Assignment (single choice)
Low speed interface	I2C	I2C4				Assignment (single choice). Used for PMIC control on ST boards.
		I2C5				Assignment (single choice)
		I2C6				Assignment (single choice)
Low speed interface *or* audio	SPI	SPI2S1				Assignment (single choice)
		SPI2S2				Assignment (single choice)
		SPI2S3				Assignment (single choice)
		SPI4				Assignment (single choice)
		SPI5				Assignment (single choice)
		SPI6				Assignment (single choice)
Low speed interface	USART	USART1				Assignment (single choice)
		USART2				Assignment (single choice)
		USART3				Assignment (single choice)
		UART4				Assignment (single choice). Used for Linux® serial console on ST boards.
						Assignment (single

Domain	Peripheral	Runtime allocation				Comment
		UART5				choice)
		USART6				Assignment (single choice)
		UART7				Assignment (single choice)
		UART8				Assignment (single choice)
Mass storage	FMC	FMC				Assignment (single choice)
Mass storage	QUADSPI	QUADSPI				Assignment (single choice)
Mass storage	SDMMC	SDMMC1				
		SDMMC2				
		SDMMC3				Assignment (single choice)
Networking	ETH	ETH				Assignment (single choice)
Networking	FDCAN	FDCAN1				Assignment (single choice)
		FDCAN2				Assignment (single choice)
Power & Thermal	DTS	DTS				
Power & Thermal	PWR	PWR				
Power & Thermal	RCC	RCC				
Security	BSEC	BSEC				
Security	CRC	CRC1				
		CRC2				
Security	CRYP	CRYP1				Assignment (single choice)
		CRYP2				
Security	ETZPC	ETZPC				

Domain	Peripheral	Runtime allocation				Comment
Security	HASH	HASH1				Assignment (single choice)
		HASH2				
Security	RNG	RNG1				Assignment (single choice)
		RNG2				
Security	TZC	TZC				
Security	TAMP	TAMP				
Trace & Debug	DBGMCU	DBGMCU				No assignment
Trace & Debug	HDP	HDP				
Trace & Debug	STM	STM				
Visual	CEC	CEC				Assignment (single choice)
Visual	DCMI	DCMI				Assignment (single choice)
Visual	DSI	DSI				
Visual	GPU	GPU				
Visual	LTDC	LTDC				

3 References

- Getting started with STM32 MPU devices#Multiple-core architecture concepts
- STM32MP15 reference manuals

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Cortex®

Operating System

Open Portable Trusted Execution Environment

Linux® is a registered trademark of Linus Torvalds.

Analog-to-digital converter. The process of converting a sampled analog signal to a digital code that represents the amplitude of the original signal sample.

Digital-to-analog converter (Electronic circuit that converts a binary number into a continuously varying value.)

Digital Filter for Sigma-Delta Modulator

voltage reference buffer (STM32 specific)

Inter-Processor Communication Controller

Hardware Semaphore

Real Time Clock

System Time Generator

System Configuration

Direct Memory Access

External Interrupt

Generic Interrupt Controller

Nested Vectored Interrupt Controller

Random Access Memory (Early computer memories generally hadserial access. Memories where any given address can be accessed when desired were then called "random access" to distinguish them from the memories where contents can only be accessed in a fixed order. The term is used today for volatile random-acces ssemiconductor memories.)

Doubledata rate (memory domain)

USB On-The-Go (Capability/type of USB port, acting primarily as USB device, to also act as USB host. Also known as USB OTG.)

USB Host (STM32 specific)

High Speed (MIPI® Alliance DSI standard)

Power Management Integrated Circuit

Ethernet

Device Tree Source (in software context) or Digital Temperature Sensor (in peripheral context)

Reset and Clock Control

Boot and Security and OTP control

Extended TrustZone Protection Controller

TrustZone® address space Controller for DDR

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Tamper

Hardware Debug Port

System Trace Module

Consumer Electronics Control (HDMI standard)

Digital Camera Memory Interface

Display Serial Interface (MIPI® Alliance standard)

Graphics Processing Units

LCD TFT Display Controller (STM32 specific)