RTC internal peripheral

Contents

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A quality version of this page, approved on *19 February 2020*, was based off this revision.

Contents

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- briefly introduce the RTC peripheral and its main features
- indicate the level of security supported by this hardware block
- explain how it can be allocated to the three runtime contexts and linked to the corresponding software components
- explain, when needed, how to configure the RTC peripheral.

2 Peripheral overview

The **RTC** peripheral is used to provide the date and clock to the application. It supports programmable alarms and wake up capabilities.

2.1 Features

Refer to STM32MP15 reference manuals for the complete list of features, and to the software components, introduced below, to know which features are really implemented.

2.2 Security support

The **RTC** peripheral is a **secure** peripheral.

3 Peripheral usage and associated software

3.1 Boot time

By default after a backup domain power-on reset (performed at boot time), all RTC registers can be read or written in both secure and non-secure modes.
In OpenSTLinux distribution, the first stage bootloader (FSBL, running in secure mode) keeps this default configuration, leaving full control to Linux® at runtime.

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3.2 Runtime

3.2.1 Overview

The **RTC** peripheral can be allocated to the Arm®Cortex®-A7 non-secure core to be used under Linux® with RTC framework.

3.2.2 Software frameworks

Domain	Peripheral	Software components		Comment
OP-TEE	Linux	STM32Cube		
Core	RTC		Linux RTC framework	

3.2.3 Peripheral configuration

The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via STM32CubeMX tool for all internal peripherals, and then manually completed (especially for external peripherals) according to the information given in the corresponding software framework article.

For Linux kernel configuration, please refer to RTC device tree configuration.

3.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- means that the peripheral can be assigned () to the given runtime context.
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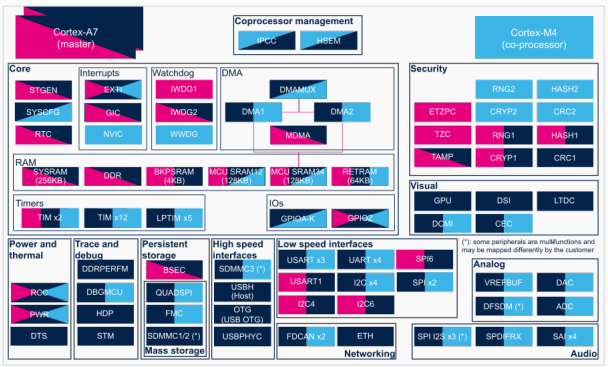

Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Core	RTC	RTC				RTC is mandatory to resynchronize STGEN after exiting low-power modes.

Real Time Clock

First Stage Boot Loader

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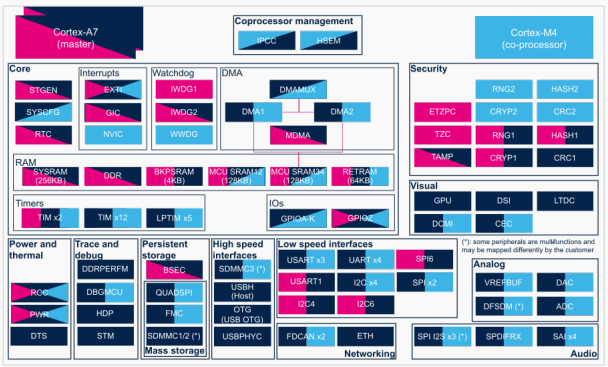

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Real Time Clock

First Stage Boot Loader

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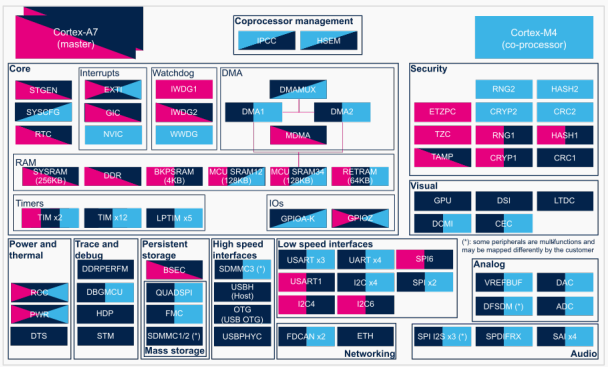

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Real Time Clock

First Stage Boot Loader

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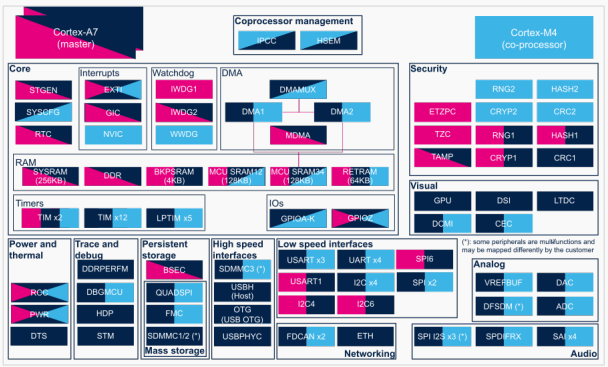

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Real Time Clock

First Stage Boot Loader

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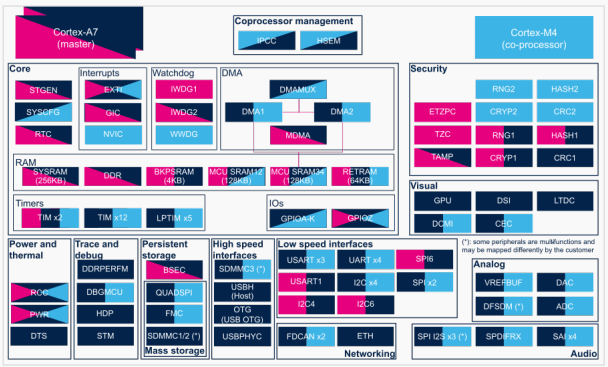

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Real Time Clock

First Stage Boot Loader

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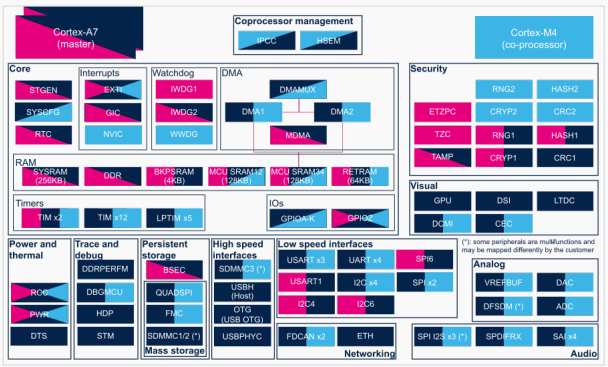

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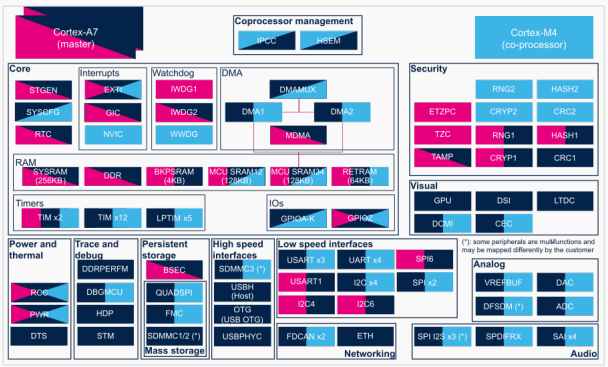

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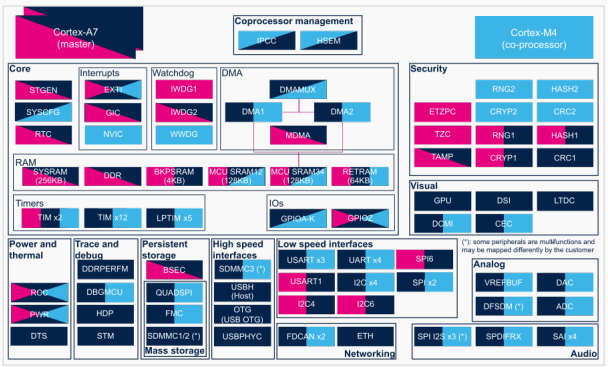

Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Core	RTC	RTC				RTC is mandatory to resynchronize STGEN after exiting low-power modes.

Real Time Clock

First Stage Boot Loader

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Cortex®

Open Portable Trusted Execution Environment

Stable: 25.09.2020 - 09:42 / Revision: 25.09.2020 - 09:36

Contents

1 Article purpose

The purpose of this article is to

- briefly introduce the RTC peripheral and its main features
- indicate the level of security supported by this hardware block
- explain how it can be allocated to the three runtime contexts and linked to the corresponding software components
- explain, when needed, how to configure the RTC peripheral.

2 Peripheral overview

The **RTC** peripheral is used to provide the date and clock to the application. It supports programmable alarms and wake up capabilities.

2.1 Features

Refer to STM32MP15 reference manuals for the complete list of features, and to the software components, introduced below, to know which features are really implemented.

2.2 Security support

The **RTC** peripheral is a **secure** peripheral.

3 Peripheral usage and associated software

3.1 Boot time

By default after a backup domain power-on reset (performed at boot time), all RTC registers can be read or written in both secure and non-secure modes.
In OpenSTLinux distribution, the first stage bootloader (FSBL, running in secure mode) keeps this default configuration, leaving full control to Linux® at runtime.

The **RTC** peripheral is able to generate two interrupts:

- A secure interrupt, connected to the Arm®Cortex®-A7 GIC, not used in OpenSTLinux distribution.
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The RTC reset occurs when the backup domain is reset. To avoid clearing the TAMP register contents, this is only done on cold boot, not on wake up.

3.2 Runtime

3.2.1 Overview

The **RTC** peripheral can be allocated to the Arm®Cortex®-A7 non-secure core to be used under Linux® with RTC framework.

3.2.2 Software frameworks

Domain	Peripheral	Software components			Comment
OP-TEE	Linux	STM32Cube			
Core	RTC		Linux RTC framework		

3.2.3 Peripheral configuration

The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via STM32CubeMX tool for all internal peripherals, and then manually completed (especially for external peripherals) according to the information given in the corresponding software framework article.

For Linux kernel configuration, please refer to RTC device tree configuration.

3.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- means that the peripheral can be assigned () to the given runtime context.
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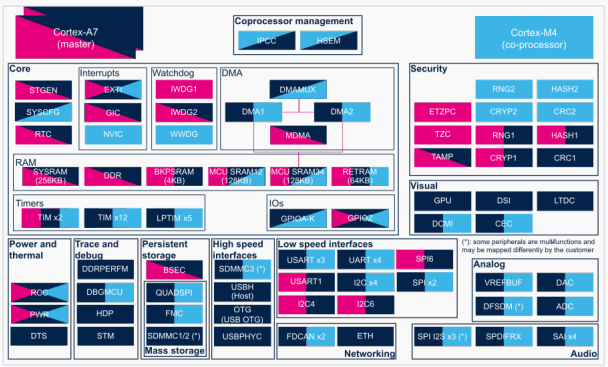

Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Core	RTC	RTC				RTC is mandatory to resynchronize STGEN after exiting low-power modes.

Real Time Clock

First Stage Boot Loader

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Open Portable Trusted Execution Environment

Stable: 23.09.2020 - 13:22 / Revision: 12.06.2020 - 13:25

Contents

1 Article purpose

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- explain how it can be allocated to the three runtime contexts and linked to the corresponding software components
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2 Peripheral overview

The **RTC** peripheral is used to provide the date and clock to the application. It supports programmable alarms and wake up capabilities.

2.1 Features

Refer to STM32MP15 reference manuals for the complete list of features, and to the software components, introduced below, to know which features are really implemented.

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The **RTC** peripheral is a **secure** peripheral.

3 Peripheral usage and associated software

3.1 Boot time

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3.2 Runtime

3.2.1 Overview

The **RTC** peripheral can be allocated to the Arm®Cortex®-A7 non-secure core to be used under Linux® with RTC framework.

3.2.2 Software frameworks

Domain	Peripheral	Software components			Comment
OP-TEE	Linux	STM32Cube			
Core	RTC		Linux RTC framework		

3.2.3 Peripheral configuration

The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via STM32CubeMX tool for all internal peripherals, and then manually completed (especially for external peripherals) according to the information given in the corresponding software framework article.

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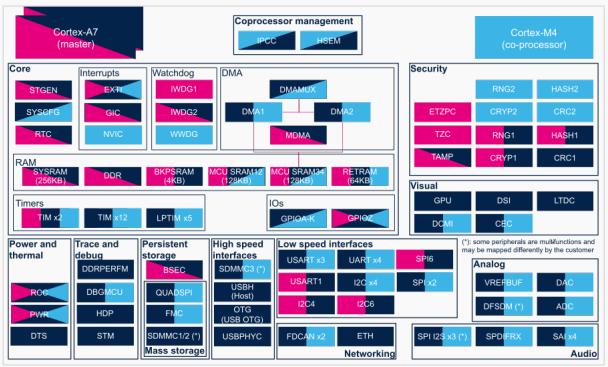

Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Core	RTC	RTC				RTC is mandatory to resynchronize STGEN after exiting low-power modes.

Real Time Clock

First Stage Boot Loader

Stable: 20.07.2021 - 09:02 / Revision: 11.03.2021 - 08:07

Contents

1 Article purpose

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3.2 Runtime

3.2.1 Overview

The **RTC** peripheral can be allocated to the Arm®Cortex®-A7 non-secure core to be used under Linux® with RTC framework.

3.2.2 Software frameworks

Domain	Peripheral	Software components			Comment
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3.2.3 Peripheral configuration

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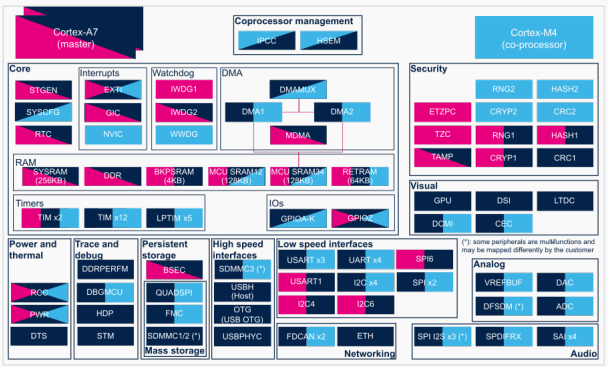

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Real Time Clock

First Stage Boot Loader

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Open Portable Trusted Execution Environment

Stable: 26.03.2021 - 11:32 / Revision: 12.03.2021 - 11:07

Contents

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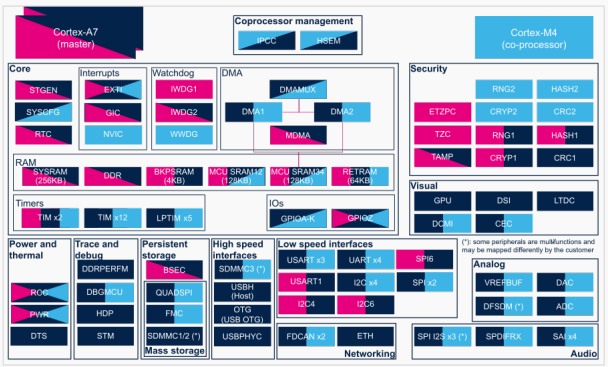

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Real Time Clock

First Stage Boot Loader

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Stable: 15.09.2021 - 06:37 / Revision: 15.09.2021 - 06:35

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3.2 Runtime

3.2.1 Overview

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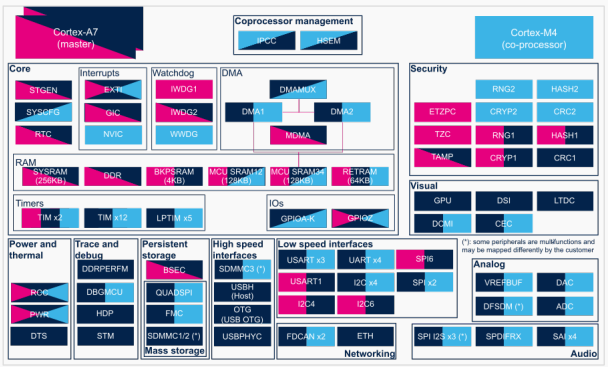

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