OTG internal peripheral

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Stable: 04.02.2020 - 16:08 / Revision: 04.02.2020 - 16:02

Template:ArticleMainWriter Template:ArticleApprovedVersion

Contents

1 Article purpose

The purpose of this article is to

- briefly introduce the OTG peripheral and its main features
- indicate the level of security supported by this hardware block
- explain how it can be allocated to the three runtime contexts and linked to the corresponding software components
- explain, when needed, how to configure the OTG peripheral.

2 Peripheral overview

The **OTG** peripheral is used to interconnect other systems with STM32 MPU devices, using USB standard.

2.1 Features

The **OTG** peripheral is a USB Dual-Role Device (DRD) controller that supports both device and host functions.
In Host mode, it supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).
In Peripheral mode, high-speed and full-speed are supported, not low-speed.
The **OTG** peripheral embeds a full-speed PHY and supports a UTMI interface connected to internal HS PHY.

The **OTG** peripheral is fully compliant with

- *On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*[1], Revision 2.0, May 8, 2009
- *Universal Serial Bus Revision 2.0 Specification*[2], Revision 2.0, April 27, 2000
- *USB 2.0 Link Power Management Addendum Engineering Change Notice to the USB 2.0 specification*[3], July 16, 2007
- *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification*[4], Version 1.05, March 29, 2001
- *UTMI+ Specification*[5], Revision 1.0, February 25, 2004

Refer to STM32MP15 reference manuals for the complete hardware feature list, and to the software components (introduced below) to know which features are supported.

2.2 Security support

The **OTG** peripheral is a **non-secure** peripheral.

3 Peripheral usage and associated software

3.1 Boot time

The OTG peripheral is used by ROM code, FSBL and SSBL in device mode (DFU) to support serial boot for flash programming with STM32CubeProgrammer.
The SSBL can use it in host mode (mass storage), for instance to boot on a kernel stored on a USB key, or after a kernel panic to perform the crash dump saving to the USB key.

3.2 Runtime

3.2.1 Overview

The OTG peripheral can be allocated to the Arm® Cortex®-A7 non-secure core to be used under Linux® with USB framework.

3.2.2 Software frameworks

Domain	Peripheral	Software frameworks	Comment
Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)	

Domain	Peripheral		Software frameworks		Comment
High speed interface	OTG (USB OTG)		Linux USB framework		

3.2.3 Peripheral configuration

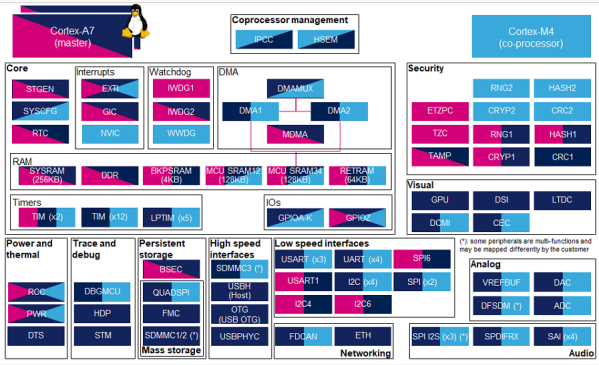
The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration by itself can be performed via the STM32CubeMX tool for all internal peripherals. It can then be manually completed (especially for external peripherals) according to the information given in the corresponding software framework article.

For Linux kernel configuration, please refer to OTG device tree configuration.

3.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- â means that the peripheral can be assigned (â) to the given runtime context.
- â is used for system peripherals that cannot be unchecked because they are statically connected in the device.



Internal peripherals

Refer to How to assign an internal peripheral to a runtime context for more information on how to assign peripherals manually or via STM32CubeMX.
The present chapter describes STMicroelectronics recommendations or choice of implementation. Additional possiblities might be described in STM32MP15 reference manuals.

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
High	OT					

Domain	Peripheral	Runtime allocation				Comment
speed interface	G (USB OTG)	OTG (USB OTG)		â		

4 References

- â On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
- â Universal Serial Bus Revision 2.0 Specification
- â ECN USB 2.0 Link Power Management Addendum
- â USB 2.0 Transceiver Macrocell Interface (UTMI) Specification
- â UTMI+ Specification