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NVIC internal peripheral



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- briefly introduce the NVIC and its main features
- indicate the level of security supported by this hardware block
- explain how the NVIC can be configured.



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## 2 Peripheral overview

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The **NVIC** is the Arm<sup>®</sup> Cortex<sup>®</sup>-M4 interrupt controller. As a result, it cannot be accessed by the Arm Cortex-A7 core.

### 2.1 Features

Refer to [STM32MP15 reference manuals](#) for the complete list of features, and to the software components, introduced below, to see which features are implemented.

### 2.2 Security support

The NVIC is a **non-secure** peripheral.



### 3 Peripheral usage and associated software

#### 3.1 Boot time

The NVIC can be configured through the STM32Cube. Refer to the [STM32MP15 interrupts](#) article for more information on the interrupt configuration strategy.

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The NVIC can be allocated only to the Arm Cortex-M4 core to be controlled in the STM32Cube by the NVIC HAL driver.

##### 3.2.2 Software frameworks

Domain	Peripheral	Software components	Comment
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Core /Interrupts	NVIC		STM32Cube NVIC driver

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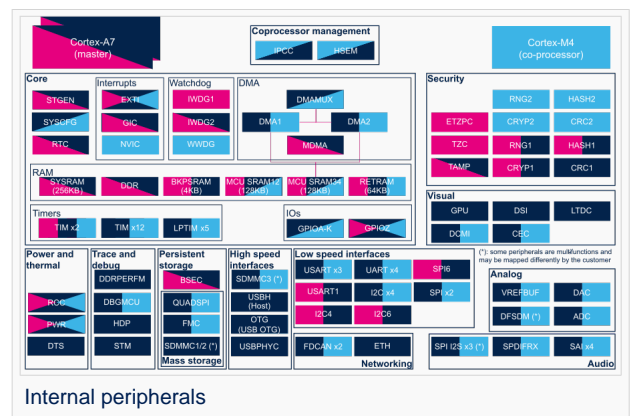
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Domain	Periphera	Runtime allocation	Comment
	Cortex-A7 secure	Cortex-A7 non-secure	Cortex-M4



Domain	Periphera	Runtime allocation			Comment
Instance	(OP-TEE)	(Linux)	(STM32Cube)		
Core /Interrupts	NVIC	NVIC			

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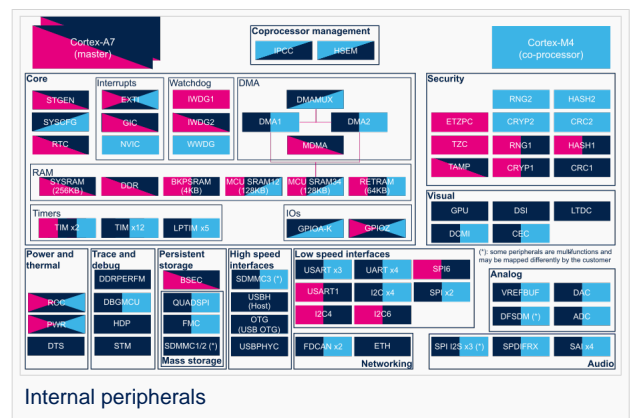
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Domain	Periphera	Runtime allocation			Comment
Instance	(OP-TEE)	(Linux)	(STM32Cube)		
Core /Interrupts	NVIC	NVIC			

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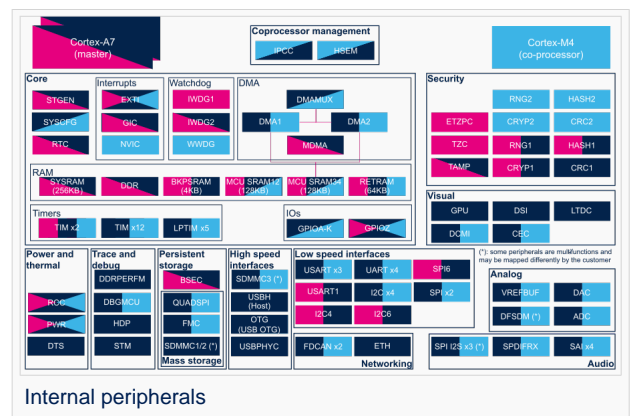
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Domain	Periphera	Runtime allocation			Comment
Instance	(OP-TEE)	(Linux)	(STM32Cube)		
Core /Interrupts	NVIC	NVIC			

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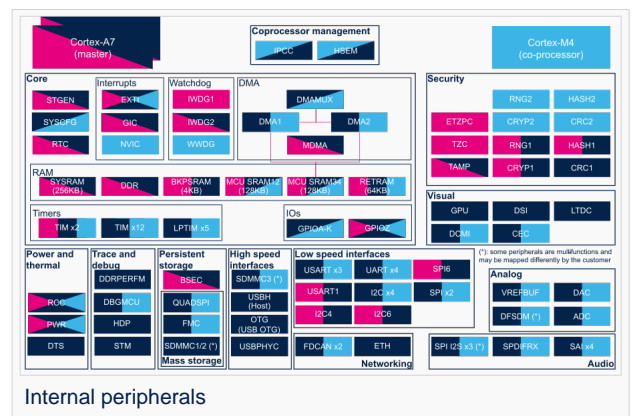
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Instance	(OP-TEE)	(Linux)	(STM32Cube)		
Core /Interrupts	NVIC	NVIC			

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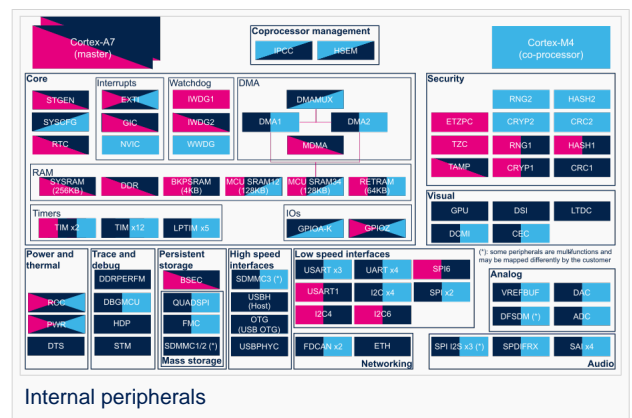
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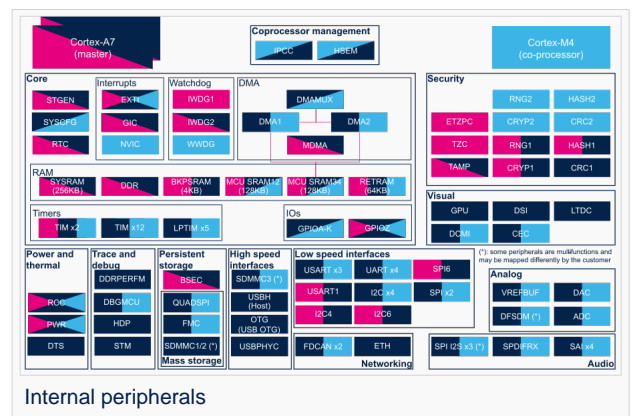
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