NVIC internal peripheral

Contents

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A quality version of this page, approved on *17 February 2021*, was based off this revision.

Contents

1 Article purpose

The purpose of this article is to:

- briefly introduce the NVIC and its main features
- indicate the level of security supported by this hardware block
- explain how the NVIC can be configured.

2 Peripheral overview

The **NVIC** is the Arm® Cortex®-M4 interrupt controller. As a result, it cannot be accessed by the Arm Cortex-A7 core.

2.1 Features

Refer to STM32MP15 reference manuals for the complete list of features, and to the software components, introduced below, to see which features are implemented.

2.2 Security support

The NVIC is a **non-secure** peripheral.

3 Peripheral usage and associated software

3.1 Boot time

The NVIC can be configured through the STM32Cube. Refer to the STM32MP15 interrupts article for more information on the interrupt configuration strategy.

3.2 Runtime

3.2.1 Overview

The NVIC can be allocated only to the Arm Cortex-M4 core to be controlled in the STM32Cube by the NVIC HAL driver.

3.2.2 Software frameworks

Domain	Peripheral	Software components	Comment
OP-TEE	Linux	STM32Cube	
Core /Interrupts	NVIC	STM32Cube NVIC driver	

3.2.3 Peripheral configuration

The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via the STM32CubeMX tool for all internal peripherals, and then manually completed (particularly for external peripherals), according to the information given in the corresponding software framework article.

3.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- means that the peripheral can be assigned () to the given runtime context.
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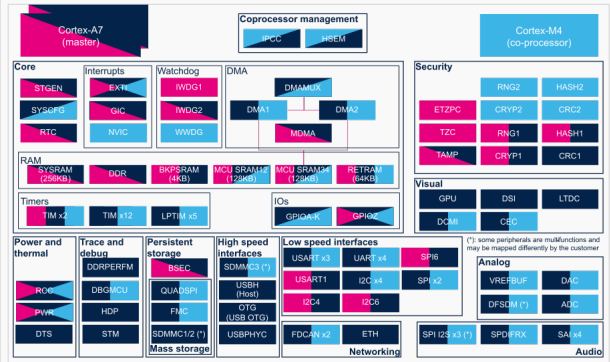
Refer to How to assign an internal peripheral to a runtime context for more information on how to assign peripherals manually or via STM32CubeMX.
The present chapter describes STMicroelectronics recommendations or choice of implementation. Additional possiblities might be described in STM32MP15 reference manuals .



Internal peripherals

Domain	Periphera l	Runtime allocation		Comment
	Cortex-A7 secure	Cortex-A7 non-secure	Cortex-M4	

Domain	Periphera	Runtime allocation				Comment
Instance	(OP-TEE)	(Linux)	(STM32Cube)			
Core /Interrupts	NVIC	NVIC				

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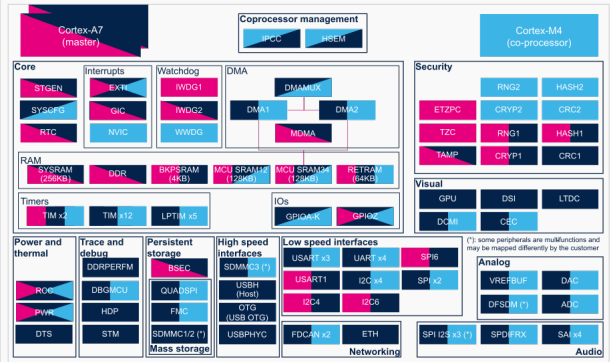

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Instance	(OP-TEE)	(Linux)	(STM32Cube)			
Core /Interrupts	NVIC	NVIC				

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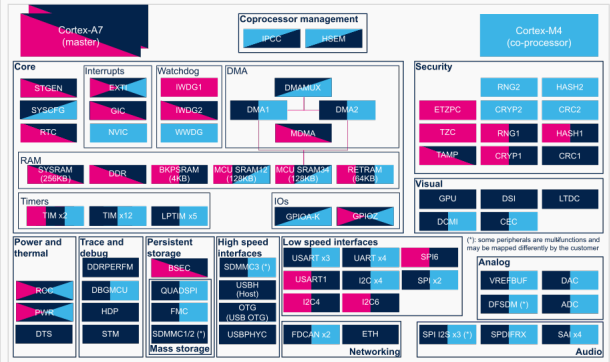

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Instance	(OP-TEE)	(Linux)	(STM32Cube)			
Core /Interrupts	NVIC	NVIC				

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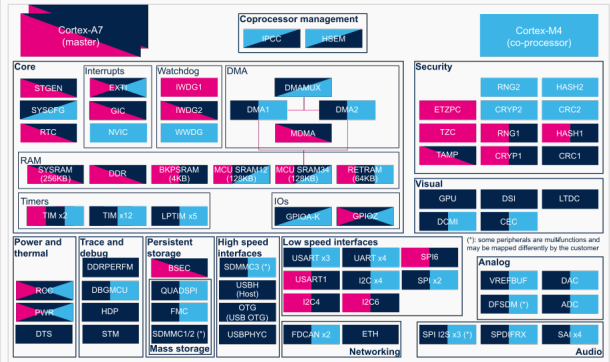

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Instance	(OP-TEE)	(Linux)	(STM32Cube)			
Core /Interrupts	NVIC	NVIC				

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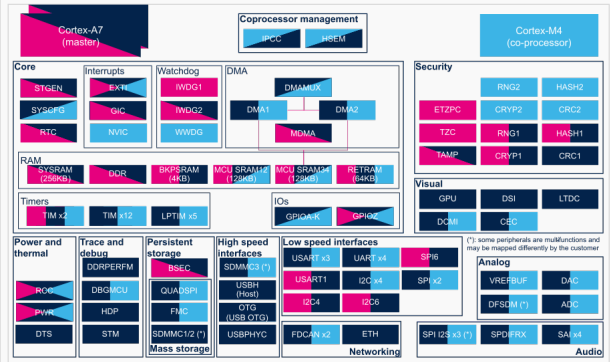

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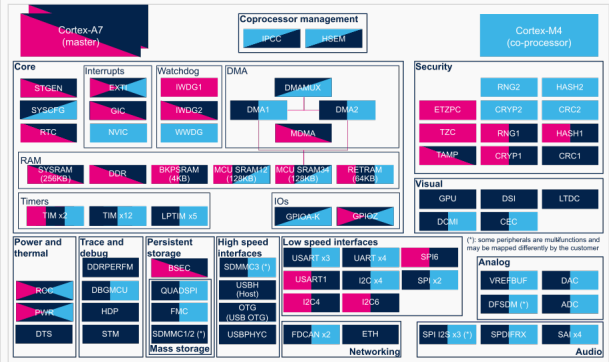

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