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IWDG internal peripheral

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Stable: 25.09.2020 - 09:42 / Revision: 25.09.2020 - 09:37

Stable: 23.06.2020 - 08:42 / Revision: 23.06.2020 - 08:37

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==Peripheral overview== The '''IWDG''' peripheral is a watchdog unit that can be used to protect application frameworks running on Cortex-A7 from endless loops. This peripheral supports an '''independent''' clocking source in order to be able to continue running even when the rest of the system is in [[Power overview|low power mode]] (STOP, STANDBY). Another important feature of this block is the '''early interrupt''' feature that allows to trigger an interrupt at a given power supply threshold before reaching the final reset: this gives the opportunity to run a recovery mechanism that will try to revive the system with minimum impact.
 ===Features=== Refer to [[STM32MP15 resources#Reference manuals|STM32MP15 reference manuals]] for the complete list of features, and to the software components, introduced below, to see which features are implemented.
 ===Security support=== IWDG1 is '''secure-aware''' (under [[ETZPC_internal_peripheral|ETZPC]] control).
 IWDG2 is '''non-secure'''. ==Peripheral usage and associated software== ===Boot time=== Pay attention to the fact that IWDG can be configured to be '''automatically active''' at startup (without any software intervention) via [[BSEC internal peripheral|BSEC]]. When this is the case, the watchdog is anyway frozen during [[STM32MP15 ROM code overview|ROM code]] execution but it will start to decrement its counter as soon as the ROM code is left so it is important to reload the watchdog from the [[Boot chains overview|boot chain]] in this case. This behavior is implemented for '''IWDG2 only''' in STMicroelectronics distribution via the [[Boot chains overview#STM32MP boot chains|trusted boot chain]] only.
 Notice also that [[BSEC internal peripheral|BSEC]] features some freeze bits that allow to '''freeze IWDG''' during platform STOP and STANDBY [[Power overview|low power]] periods, avoiding to have to wake up (via [[RTC internal peripheral|RTC]]) for the only purpose of reloading the watchdog. ===Runtime=== ====Overview==== IWDG1 can be allocated to the Cortex-A7 secure to be used in the secure context by the customer application: this instance is not supported in STMicrolectronics distribution.
 IWDG2 can be allocated to the Cortex-A7 non-secure to be used with Linux [[Watchdog overview|watchdog]] framework. In this configuration, the secure monitor (from [[OP-TEE overview|OP-TEE]] -if present- or [[TF-A overview|TF-A]]) is able to receive IWDG early interrupts that can be used in a tentative to reset the Cortex-A7 without interfering with Cortex-M4 execution. ====Software frameworks==== {{:Internal_peripherals_software_table_template}} | Core/Watchdog | [[IWDG internal peripheral|IWDG]] | [[TF-A overview#BL32|TF-A]] | [[Watchdog overview|Linux watchdog framework]] | | |- |} ====Peripheral configuration==== The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via the [[STM32CubeMX]] tool for all internal peripherals, and then manually completed (particularly for external peripherals), according to the information given in the corresponding software framework article. ====Peripheral assignment==== {{:Internal_peripherals_assignment_table_template}} <onlyinclude> | rowspan="2" | Core /Watchdog | rowspan="2" | [[IWDG internal peripheral|IWDG]] | IWDG1 | | | | |- | IWDG2 | | | | Shared (none or both): * Cortex-A7 non secure for reload * Cortex-A7 secure for early interrupt handling |- </onlyinclude> |} <noinclude> [[Category: Watchdog peripherals]] {{PublicationRequestId | 8856 | 2018-09-21 | BrunoB}} {{ArticleBasedOnModel| Internal peripheral article model}} {{ReviewsComments|JCT 1840: alignment needed with the last version of the model [[Contributors:Internal peripheral article model]]
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