BKPSRAM internal memory

BKPSRAM internal memory

Stable: 04.02.2020 - 15:59 / Revision: 04.02.2020 - 15:55

Contents

1 Peripheral overview

The **BKPSRAM** internal memory is 4 Kbytes wide and is located in the VSW power domain, allowing it to be supplied during Standby low power mode, or to be switched off.

1.1 Features

Refer to STM32MP15 reference manuals for the complete feature list, and to the software components introduced below, to see which features are currently implemented.

1.2 Security support

The BKPSRAM is a **secure** peripheral (under ETZPC control).

2 Peripheral usage and associated software

2.1 Boot time

The BKPSRAM internal memory is not used during a cold boot or a wake up from Standby with DDR OFF.

The BKPSRAM internal memory is used by the runtime secure monitor (from the FSBL or the OP-TEE secure OS) during wake-up from Standby low power mode with the DDR in Self-Refresh mode. In that case, the BKPSRAM internal memory contains the secure context that has to be restored before jumping back to Linux execution, in DDR.

2.2 Runtime

2.2.1 Overview

The BKPSRAM peripheral can be allocated to:

- the Arm® Cortex®-A7 secure to be used under PSCI [1] secure services (from the FSBL or OP-TEE secure monitor) to save the secure context before entering STANDBY low power mode with DDR in Self-Refresh mode. This is the default assignement.

or

- the Cortex-A7 non-secure to be used under Linux® as reserved memory, for instance.

2.2.2 Software frameworks

Do	Peri	Software frameworks			Comment
mai n Cor tex -A7 sec ure (O P- TE E)	Cor tex -A7 no n- sec ure (Li nux)	Cortex-M4 (STM32Cube)			
Co re/ R A M	BK PS R A M	TF-A overview	Linux reserved memory		

2.2.3 Peripheral configuration

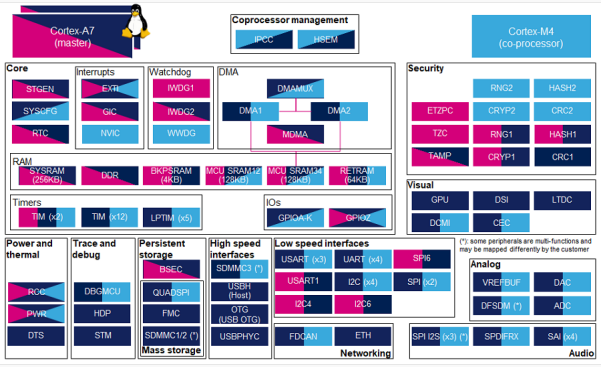
The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration by itself can be done via the STM32CubeMX tool for all internal peripherals, and can then be manually be completed (particularly for external peripherals), according to the information given in the corresponding software framework article.

2.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by STM32 MPU Embedded Software:

- means that the peripheral can be assigned () to the given runtime context.
- is used for system peripherals that cannot be unchecked because they are statically connected in the device.

Refer to How to assign an internal peripheral to a runtime context for more information on how to assign peripherals manually or via STM32CubeMX.
The present chapter describes STMicroelectronics recommendations or choice of implementation. Additional possiblities might be described in STM32MP15 reference manuals.



Internal peripherals

Domain	Peripheral	Runtime allocation				Comment
Instance	Cortex-A7 secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
Core/RAM	BKPSRAM	BKPSRAM				Assignment (single choice)

3 References

- http://infocenter.arm.com/help/topic/com.arm.doc.den0022d/Power_State_Coordination_Interface_PDD_v1_1_DEN0022D.pdf

Power State Coordination Interface

Doubledata rate (memory domain)

Open Portable Trusted Execution Environment

Random Access Memory (Early computer memories generally hadserial access. Memories where any given address can be accessed when desired were then called "random access" to distinguish them from the memories where contents can only be accessed in a fixed order. The term is used today forvolatile random-accesssemiconductor memories.)