



STM32MP15 microprocessor



A quality version of this page, approved on 21 February 2020, was based off this revision.

In a first part, this article shows the STM32MP157 line **part number codification** and **block diagram**. STM32MP157 belongs to STM32MP1 Series (refer to the list of part numbers provided below).

The second part of this article digs into technical aspects, and provides entry points to:

- STM32MP15 **documentation**
- articles dedicated to **Internal peripherals** that make the transition towards the software frameworks required to control these peripherals
- the list of **boards** supporting STM32MP15 devices
- the supported **software distributions**, that can be downloaded into the STM32MP15 device.

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1 Introduction

STM32MP15 microprocessors are based on the Arm[®]Cortex[®]-A7 dual core. They support Trustzone mode for secure operations, a **Vivante GPU** and an Arm[®]Cortex[®]-M4 coprocessor.

Arm[®] Cortex[®]-M4 coprocessor and its peripheral set are directly inherited from the STM32 MCU family ^[1].



2 Part number codification

The table below shows the STM32MP15 microprocessor different part numbers available, together with their corresponding internal peripherals, security options and packages.

2.1 STM32MP15x lines

	Cortex-A7	Cortex-M4	GPU	Display	CAN
STM32MP151	Single	Yes	No	TFT	No
STM32MP153	Dual	Yes	No	TFT	Yes
STM32MP157	Dual	Yes	Yes	TFT/DSI	Yes

2.2 Security and Cortex-A7 frequency

	Security	Cortex-A7 frequency
STM32MP15xA	Basic	650 MHz ^[2]
STM32MP15xC	Secure boot + Cryptography (CRYP)	650 MHz ^[2]
STM32MP15xD	Basic	800 MHz ^{[2][3]}
STM32MP15xF	Secure boot + Cryptography (CRYP)	800 MHz ^{[2][3]}

2.3 Packages

STM32MP15xxAA	TFBGA448 18x18
STM32MP15xxAB	LFBGA354 16x16
STM32MP15xxAC	TFBGA361 12x12
STM32MP15xxAD	TFBGA257 10x10

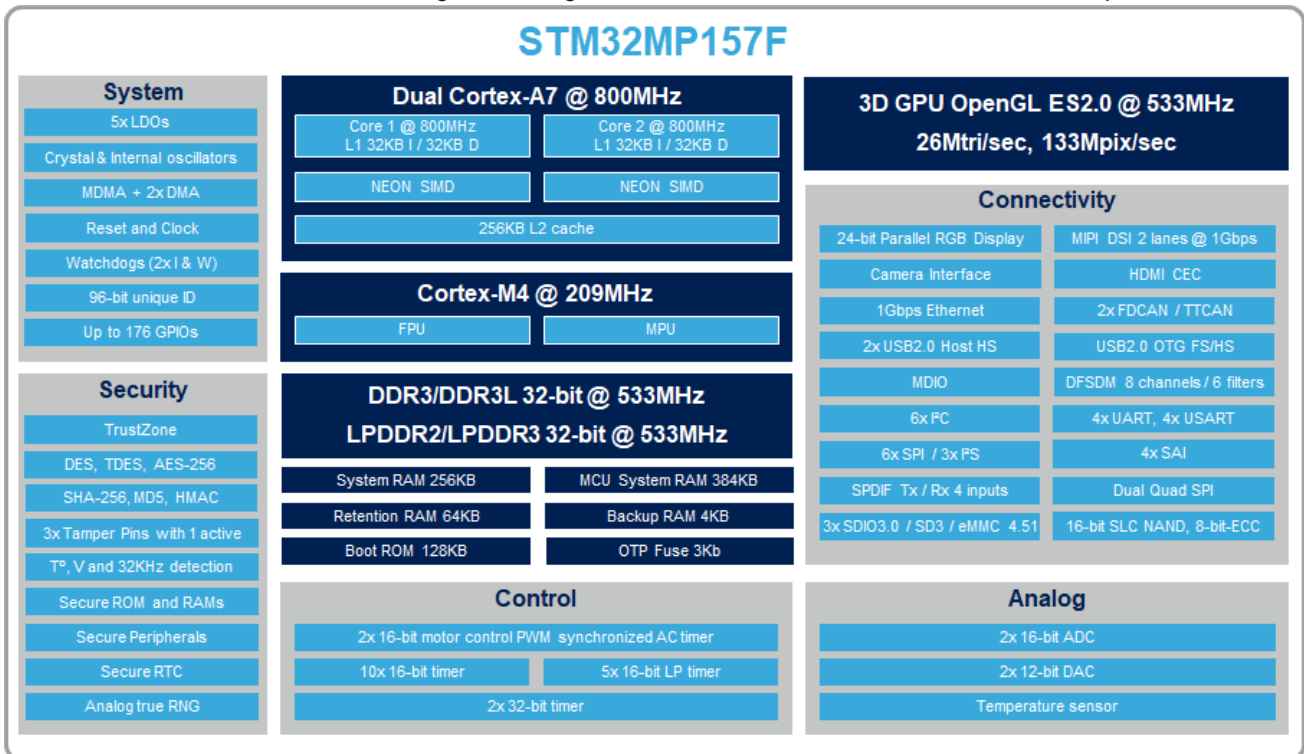
2.4 Junction temperature

STM32MP15xxxx1	- 20 to + 105 °C ^{[2][3]}
STM32MP15xxxx3	- 40 to + 125 °C ^[2]



3 Block diagram

Here below is the STM32MP157F block diagram offering the richest features set of the STM32MP15 microprocessor.





4 Technical documentation

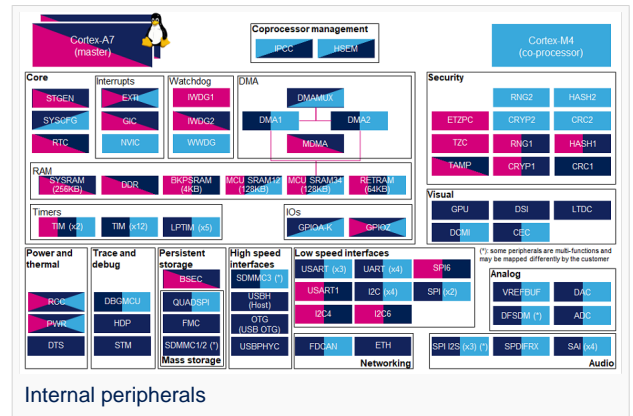
- [STM32MP15 Reference Manual](#): device and internal peripheral user specifications
- [STM32MP15 Datasheet](#): electrical characteristics, package and pinout descriptions



5 Internal peripherals

STM32MP15 peripherals overview article gives a description of all the internal peripherals available on STM32MP15 devices, with direct links to the articles where you can find:

- an overview of each peripheral
- the list of instances available for each peripheral type,
- information on the way each instance can be shared between Arm® Cortex®-A7 and Cortex®-M4 cores,
- direct links to the software frameworks used to control the peripheral from different Arm® cores and security modes such as Cortex®-A7 non secure, Cortex®-A7 secure or Cortex®-M4 (non secure).







6 How to get further with STM32MP15 ecosystem

6.1 Boards

The list of boards that integrate STM32MP15 devices can be found in [STM32MP15 boards](#) article.

6.2 Supported software distributions

 STM32MPU Embedded Software distribution	 STM32MPU Embedded Software distribution for Android
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Click the links above to find information on:

- [Distribution composition and associated software architecture](#)
- [Associated release notes](#)



7 References and foot notes

- STM32 MCU family
- 2.02.12.22.32.42.5 Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard. Refer to the [STM32MP15 Datasheet](#) and [AN5438](#) for further information.
- 3.03.13.2 800 MHz part numbers are only available with '1' as junction temperatures range suffix (- 20 to + 105 °C).

Graphics Processing Units

Microcontroller Unit (MCUs have internal flash memory and are intended to operate with a minimum amount of external support ICs. They commonly are a self-contained, system-on-chip (SoC) designs.)

Controller Area Network (robust bus mainly used for automotive applications)

Display Serial Interface (MIPI[®] Alliance standard)