

I2C internal peripheral

Contents

1	Article purpose	2
2	Peripheral overview	3
2.1	Features	3
2.2	Security support	3
3	Peripheral usage and associated software	4
3.1	Boot time	4
3.2	Runtime	4
3.2.1	Overview	4
3.2.2	Software frameworks	4
3.2.3	Peripheral configuration	4
3.2.4	Peripheral assignment	5
4	References	7

1 Article purpose

The purpose of this article is to:

- briefly introduce the I2C peripheral and its main features
- indicate the level of security supported by this hardware block
- explain how each instance can be allocated to the three runtime contexts and linked to the corresponding software components
- explain, when necessary, how to configure the I2C peripheral.

2 Peripheral overview

The I2C bus interface serves as an interface between the microcontroller and the serial I2C bus.

It provides multi-master capability, and controls all I2C bus-specific sequencing, protocol, arbitration and timing.

The I2C controller allows to be a slave as well if need be.

It is also SMBus 2.0 compatible.

For more information about I2C please refer to this link: [I2C wikipedia](#)^[1] or [i2c-bus.org](#)^[2]

For more information about SMBus please refer to this link: [SMBus wikipedia](#)^[3] or [i2c-bus.org](#)^[4]

2.1 Features

Here are the main features:

- Multi-master
- Standard (100 KHz) and fast speed modes (400 KHz and Plus 1 MHz)
- I2C 10-bit address
- I2C slave capabilities (programmable I2C address)
- DMA capabilities
- SMBus 2.0 compatible
 - Standard bus protocol (quick command; byte, word, block read/write)
 - Host notification
 - Alert

Refer to the [STM32MP15 reference manuals](#) for the complete list of features, and to the software components, introduced below, to see which features are implemented.

2.2 Security support

- There are six I2C instances.
 - I2C instances 1, 2, 3 and 5 are **non-secure**.
 - I2C instances 4 and 6 can be **secure** (under [ETZPC](#) control).

3 Peripheral usage and associated software

3.1 Boot time

The I2C peripheral is usually not used at boot time. But it may be used by the SSBL and/or FSBL (see [Boot chains overview](#)), for example, to configure a PMIC (see [PMIC hardware components](#)), or to access data stored in an external EEPROM.

3.2 Runtime

3.2.1 Overview

I2C4&6 instances can be allocated to:

- the Arm[®] Cortex[®]-A7 secure core to be controlled in OP-TEE by the [OP-TEE I2C driver](#)

All I2C instances can be allocated to:

- the Arm[®] Cortex[®]-A7 non-secure core to be controlled in U-Boot or Linux[®] by the [I2C framework](#)

All but I2C4&6 instances can be allocated to:

- the Arm[®] Cortex[®]-M4 to be controlled in STM32Cube MPU Package by [STM32Cube I2C driver](#)

Chapter [Peripheral assignment](#) describes which peripheral instance can be assigned to which context.

3.2.2 Software frameworks

Dom	Peri	Software frameworks			Comment
Main Cortex-A7 non-secure (OP-TEE)	Cortex-A7 non-secure (Linux)	Cortex-M4 (STM32Cube)			
		Low speed interface	I2C	OP-TEE I2C driver	I2C Engine framework

3.2.3 Peripheral configuration

The configuration is applied by the firmware running in the context to which the peripheral is assigned. The configuration can be done alone via the [STM32CubeMX](#) tool for all internal peripherals, and then manually completed (particularly for external peripherals), according to the information given in the corresponding software framework article.

For Linux® kernel configuration, please refer to [I2C configuration](#).

Please refer to [I2C device tree configuration](#) for detailed information on how to configure I2C peripherals.

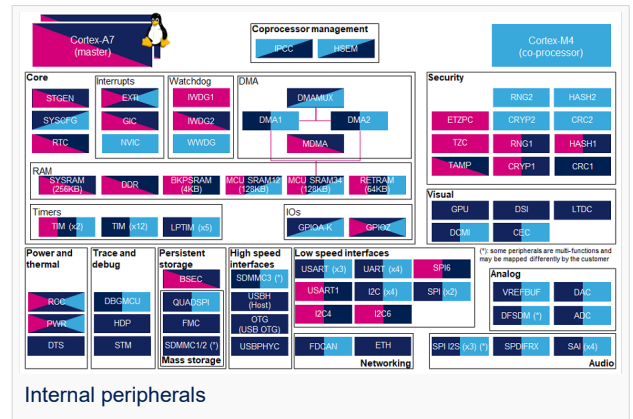
3.2.4 Peripheral assignment

Check boxes illustrate the possible peripheral allocations supported by [STM32 MPU Embedded Software](#):

- means that the peripheral can be assigned () to the given runtime context.
- is used for system peripherals that cannot be unchecked because they are statically connected in the device.

Refer to [How to assign an internal peripheral to a runtime context](#) for more information on how to assign peripherals manually or via [STM32CubeMX](#).

The present chapter describes STMicroelectronics recommendations or choice of implementation. Additional possibilities might be described in [STM32MP15 reference manuals](#).



Do	Per	Runtime allocation				Commen
mai	ion Cort era ex- A7 - TEE)	Cortex-A7 non-secure (Linux)		Cortex-M4 (STM32Cube)		
anc		I2C1	<input type="checkbox"/>	<input type="checkbox"/>	Assignme nt (single choice)	
spe		I2C2	<input type="checkbox"/>	<input type="checkbox"/>	Assignme nt (single choice)	
ed		I2C3	<input type="checkbox"/>	<input type="checkbox"/>	Assignme nt (single choice)	
inte	I2C				Assignme nt (single choice). Used for PMIC	

Do	Per	Runtime allocation				Commen
mai n e	iph era l	I2C4	<input type="checkbox"/>	<input type="checkbox"/>		control on ST boards .
		I2C5		<input type="checkbox"/>	<input type="checkbox"/>	Assignme nt (single choice)
		I2C6	<input type="checkbox"/>	<input type="checkbox"/>		Assignme nt (single choice)

4 References

- ↑ <http://en.wikipedia.org/wiki/I2C>
- ↑ <https://www.i2c-bus.org/specification/>
- ↑ https://en.wikipedia.org/wiki/System_Management_Bus
- ↑ <https://www.i2c-bus.org/smbus/>

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved