



How to change the CPU frequency



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1 Purpose

This article explains how to change the CPU **operating point** (also known as OPP). An operating point corresponds to the **frequency** of the processor and the **voltage** that needs to be supplied to sustain it.



2 Hardware side

On STM32MP1 Series products, the Cortex-A7 core is:


- clocked by PLL1 from the RCC internal peripheral. The PLL1P output **frequency** can be directly propagated to the core, or it can go through an intermediate MPUDIV divider
- supplied with VDDcore **voltage**.


The **part number** tells which devices can be clocked up to 800 MHz, with associated usage conditions. Otherwise, the frequency must be kept below 650 MHz.



3 Software side

3.1 For ecosystem release v1.2.0

The ecosystem release v1.2.0  is backward compatible with the previous deliveries, so it is still possible to set the CPU **frequency** in the TF-A device tree, as described in the paragraph below. If your **part number** supports up to 800 MHz, ensure that the VDDcore minimum **voltage** is increased from 1.2V to 1.35 V while running above 650 MHz; this is done in the **regulators** node of the board device tree.

By default however, the ecosystem release v1.2.0  does not set any configuration for PLL1 in the FSBL (TF-A). Instead, TF-A automatically selects the operating point that is suitable for the current **part number** according to the OPP table code below (embedding **frequency** and **voltage** couples) defined in the SOC device tree `fdts/stm32mp157c.dtsi`.

```
cpu0_opp_table: cpu0-opp-table {
    compatible = "operating-points-v2";
    opp-shared;

    opp-650000000 {
        opp-hz = /bits/ 64 <650000000>;
        opp-microvolt = <1200000>;
        opp-supported-hw = <0x1>;
    };
    opp-800000000 {
        opp-hz = /bits/ 64 <800000000>;
        opp-microvolt = <1350000>;
        opp-supported-hw = <0x2>;
    };
};
```

Notes:

- The operating point supported by devices supporting above 650 MHz (and up to 800 MHz) is identified by the **opp-supported-hw** property set to 0x2.
- This same OPP table must also be present in the Linux SOC device tree `arch/arm/boot/dts/stm32mp157c.dtsi`.
- It is possible to do a mix, specifying the PLL1 configuration (without an OPP table) in the TF-A device tree, whereas Linux uses the OPP table to increase the CPU frequency, once started.
- This description is valid for cold boot, but also when coming back from Standby low power mode.
- During cold boot, TF-A computes and saves the PLL1 settings for all operating points available in the device tree in compliance with the hardware capabilities. These saved parameters are used later to increase the performance of the system-state transitions.

3.2 For ecosystem release v1.1.0

The Cortex-A7 core frequency is selected at boot time, by the FSBL (TF-A), following the Clock device tree configuration - Bootloader specific syntax. The frequency is set to 650 MHz by default, as shown in STM32MP15 clock tree. This configuration is set in the TF-A device tree, for instance `fdts/stm32mp157a-dk1.dts` file for STM32MP157C-DK1 board.

```
&rcc {
    ...
    /* VCO = 1300.0 MHz => P = 650 (CPU) */
    pll1: st,pll@0 {
```



```
        cfg = < 2 80 0 0 0 PQR(1,0,0) >;  
        frac = < 0x800 >;  
    };  
    ...  
};
```

The user can reduce this frequency by changing the above configuration, either manually or via the [STM32CubeMX](#) graphical user interface that allows generation of the corresponding device tree file.

Central processing unit

Operating Performance Point ([link to voltage and frequency scalings](#))

Trusted Firmware for Arm Cortex-A

First Stage Boot Loader